Response to Arguments

1. Applicant's arguments filed 7/2/2009 have been fully considered but they are not persuasive.

   a. Regarding **claim 1**, the applicant contends the prior art, Johnson et al in view of McCullagh et al, fails to disclose the limitation "a processor coupled to the oscillator, wherein the processor is further coupled to receive a status message from a source of the reference clock signal indicative of a quality level of the reference clock signal."

      The examiner respectfully disagrees. Fig. 2 of Johnson et al shows a monitor, label 26, for controlling the switch, label 30. Col. 5, lines 20-32 discloses "A monitor 26 monitors the input reference frequency 10. If the input reference frequency is accurate to within the desired range (approximately plus or minus 15 ppm) then the VCO 29 is phase locked to the reference input 10 so that the output 28 is in phase with the input reference. A monitor 26 constantly tests both the presence and accuracy of the input reference frequency 10. If the input signal is lost or becomes invalid, monitor 26 outputs a control signal on line 31 to couple switch 30 to the internal frequency reference of the clock holdover circuit of the present invention." Johnson et al discloses the monitor component tests for accuracy and presence of the input reference frequency 10, which indicates a status message or the status of the input reference frequency is determined and produced. The status of the input reference frequency indicates the quality level or accuracy of the reference clock signal or

the input reference frequency. Fig. 3a, labels 58 and 69 show the components

of the monitor. Label 60 shows the signal outputted when the reference input

signal is found to be invalid. Fig. 3a shows the switch controller for receiving the

reference failed message and outputting a control signal to control the switch,

label 30, wherein the message indicates the validity or the quality level of the

reference input signal as discussed in Col. 5, lines 20-32 and Fig. 2.

b. Regarding **claims 2,4-5,7-10,12-13,15-17,20-22,24-26,28,30-34**, such claims

either dependents, wherein the independent claim have the same arguments as

stated for claim 1. Please refer to the rebuttal of claim 1.

c. Based on the rebuttal above, the rejection stands as previously stated. Please

see the rejection below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set
forth in section 102 of this title, if the differences between the subject matter sought to be patented and
the prior art are such that the subject matter as a whole would have been obvious at the time the
invention was made to a person having ordinary skill in the art to which said subject matter pertains.
Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 1,4,5,7,8,9,26,28,33,34**, are rejected under 35 U.S.C. 103(a) as being

unpatentable over Johnson et al (US Patent No.: 4849993) in view of McCullagh et

al (US Publication No.: 20020022465).

a. **Claims 1,4,5,9**,

i.   Johnson et al discloses

- "a phase comparator having a first input for receiving a reference clock signal, a second input for receiving a feedback signal, and an output for providing an error signal" (Fig. 2, label 11)

- "a device having an input for receiving the error signal and an output for providing a control signal" (Fig. 2, label 50)

- "an oscillator having all input for receiving the control signal and an output for providing a timing signal, wherein the feedback signal is derived from the timing signal" (Fig. 2, label 29)

- "a processor coupled to the oscillator, wherein the processor is further coupled to receive a status message from a source of the reference clock signal indicative of a quality level of the reference clock signal" or "a processor coupled to the oscillator, wherein the processor is further coupled to receiver status messages from respective sources of the primary reference clock signal and at least one secondary reference clock signal" (Fig. 2, label 26, Col. 5, lines 20-32 discloses the input frequency signal is checked to determine if the reference signal is within the range. If not, whether falling below or above the range, the PLL will be placed in holdover. Fig. 2, label 10 is the status message is based on the reference clock signal used to determine the state of the PLL. Fig. 3a, labels 58,69 shows the status message, ref fail, is received by the controller, label 69, for controlling the switch, label 30, wherein the switch controller is part of the processor found in Fig. 2, label 10

(monitor). Fig. 3a, labels 10a and 10b show the primary and secondary

reference clock signal.) and

- "the processor places the phase locked loop in the holdover condition

    when a quality level of the reference clock signal indicated by the status

    message is less than an expected quality level of the phase locked loop

    in the holdover condition" (Col. 5, lines 20-32 discloses the input

    frequency signal is checked to determine if the reference signal is within

    the range. If not, whether falling below or above the range, the PLL will

    be placed in holdover.)

ii.   Johnson et al fails to disclose a loop filter.

iii.   McCullagh et al discloses a loop filter used within the PLL. (Fig. 4, label

       410) It would have been obvious to one skilled in the art to incorporate a

       loop filter in the PLL as disclosed by McCullagh et al into Johnson et al's

       invention so to control the VCO to determine the output of the VCO, which

       allows for more efficient synchronization of the input signals.

iv.   Johnson et al fails to disclose a loop filter and machine readable memory.

v.   McCullagh et al discloses a memory coupled to the processor (paragraph

       131), wherein the memory has instructions stored, wherein the instructions

       stored on the memory are capable of causing the processor (paragraph

       131) Although McCullagh et al does not explicitly state a machine- readable

       medium for placing the PLL in holdover condition, a instruction stored in a

       machine-readable medium to control processor is a well known. Since

Johnson et al discloses a processor for monitoring holdover conditions and placing the PLL in holdover, it would have been obvious to one skilled in the art to incorporate a machine readable medium for storing instructions based on designer's choice and to control the system to perform the required instructions or tasks so to provide better and more efficient synchronization of the input signals.

b. **Claim 2**,

   i.   Johnson et al discloses "the processor to selectively place the phase locked loop in the holdover condition in response to the status message regardless of a validity of the reference clock signal". (Col. 6, lines 20-40 discloses the monitor component checks for accuracy of the signal prior to selecting 10a for 10b. Col. 5, lines 20-32 indicates if the system is not within the desired range, the system will go into holdover.)

   ii. Johnson et al fails to discloses "the instructions stored on the machine-readable medium are capable of causing the processor" to place the PLL in holdover. McCullagh et al discloses software is stored in memory. (paragraph 131) It is well known in the art that software can be used to control the PLL. Since Johnson et al discloses a processor for monitoring holdover conditions and placing the PLL in holdover, it would have been obvious to one skilled in the art to incorporate a machine readable medium for storing instructions based on designer's choice and to control the

system to perform the required instructions or tasks so to provide better and more efficient synchronization of the input signals.

c. **Claim 7**, Johnson et al discloses "the expected quality level is at least a Stratum 2 level". (Col. 4, lines 36-43 indicates the Stratum level and the range in which the Stratum level would indicate the input signal.)

d. **Claim 8**, Johnson et al discloses "the instructions stored on the machine-readable medium are capable of causing the processor to monitor the status message and to place the phase locked loop in the holdover condition if the quality level indicated by the status message is below the target quality level when the reference clock signal is valid". (Col. 5, lines 20-32 discloses the input frequency signal is checked to determine if the reference signal is within the range. If not, whether falling below or above the range, the PLL will be placed in holdover.)

e. **Claims 26,28,33,34**,

   i.   Johnson et al discloses

   - "during a time when a primary reference clock signal is valid and has an indicated quality level at or above a target level" (Col. 6, lines 12-35 discloses selecting a reference signal. The monitor would determine the accuracy of reference 10a and 10b.)

   - "generating a first error signal indicative of a phase relationship between the primary reference clock signal and a first feedback signal" (Fig. 2, label 11)

- "generating the timing signal in response to the first control signal" (Fig. 2, label 29) and

- "deriving the first feedback signal from the timing signal" (Fig. 2, label 28)

- "during a time when the primary reference clock signal is failed or has an indicated quality level below the target level, and when a secondary reference clock signal is valid and has an indicated quality level at or above the target level" (Col. 6, lines 12-35 discloses selecting a reference signal. The monitor would determine the accuracy of reference 10a and 10b.)

- "generating a second error signal indicative of a phase relationship between the secondary reference clock signal and a second feedback signal" (Fig. 2, label 11)

- "generating the timing signal in response to the second control signal" (Fig. 2, label 28) and

- "deriving the second feedback signal from the timing signal" (Fig. 2, label 28) and

- "during a time when each reference clock signal is failed or has an indicated quality level below the target level" (Col. 5, lines 20-32 discloses the input frequency signal is checked to determine if the reference signal is within the range. If not, whether falling below or above the range, the PLL will be placed in holdover.)

- "generating a holdover control signal" (Col. 5, lines 20-32 discusses the holdover conditions and placing the PLL in holdover. To do so, a signal must be generated in order to place the PLL in holdover and indicate to other components the PLL is in holdover.) and

- "generating a timing signal in response to the holdover control signal" (Fig. 2, label 28)

- "wherein the method is performed in the order presented". (Fig. 2 shows the process and Col. 5 and 6 discusses the procedure.)

- "wherein the indicated quality level of at least one of the primary reference clock signal and the secondary reference clock signal is determined based at least in part on a status messages received from respective sources of the primary reference clock signal and the secondary reference clock signal. (Col. 6, lines 12-41 describes the secondary and primary reference clock. Col. 5, lines 20-45 describes the process of determining the status of the PLL based on the reference clock signal, label 10. Fig. 3, label 10a and 10b are the primary and secondary reference clock signals. Fig. 3a, labels 58,69 shows the status message, ref fail, is received by the controller, label 69, for controlling the switch, label 30, wherein the switch controller is part of the processor found in Fig. 2, label 10 (monitor).)

    ii.   Johnson et al fails to disclose a filter within the process.

    iii.   McCullagh et al discloses a loop filter used within the PLL. (Fig. 4, label

410) It would have been obvious to one skilled in the art to incorporate a

loop filter in the PLL as disclosed by McCullagh et al into Johnson et al's

invention so to control the VCO to determine the output of the VCO, which

allows for more efficient synchronization of the input signals.

3. **Claims 10,12,13,15** are rejected under 35 U.S.C. 103(a) as being unpatentable

over Johnson et al (US Patent No.: 4849993) in view of McCullagh et al (US

Publication No.: 20020022465), further in view of Ham, III (US Publication No.:

20020080901)

    a. **Claim 10** inherits all the limitations of claim 1, but claim 1 does not recite a

receiver, a framer and a prescaler. Ham, III discloses a cascaded parallel phase

locked loop comprising a receiver (Fig. 1), a framer for locating a frame pulse

and generating a reference clock signal from the recovered clock signal and

data signals (Fig. 4, label 60, paragraph 37) and a prescaler coupled between

the framer and PLL. (Fig. 4, labels 60,62 and Fig. 5, labels 64,66) It would be

obvious to one skilled in the art to incorporate a framer as disclosed by Ham, III

into Johnson et al's invention to provide a reference clock signal to the PLL,

wherein the reference clock signal is geared towards the information received

by the receiver, thus the PLL is synchronizing the clock signal pertaining to the

information that needed within the system. It would have been obvious to one

skilled in the art at the time of the invention to incorporate the use of a prescalar

as disclosed by Ham, III into Johnson et al's invention so to reduce the input

clock so to allow the PLL so synchronize the input clock more accurately.

b. **Claim 12** recites similar claims as claims 1 and 10. Such claims are rejected as

stated in claims 1 and 10.

c. **Claim 13**,

i.   Johnson et al discloses "the processor to monitor the status message and

to place the phase locked loop in the holdover condition if the quality level

indicated by the status message is below the target quality level when the

reference clock signal is valid". (Col. 5, lines 20-32 discloses the input

frequency signal is checked to determine if the reference signal is within the

range. If not, whether falling below or above the range, the PLL will be

placed in holdover. The column also discloses the monitor checks for

validity of the signal.)

ii.   Johnson et al fails to discloses "the instructions stored on the machine-

readable medium are capable of causing the processor" to place the PLL in

holdover. McCullagh et al discloses software is stored in memory.

(paragraph 131) It is well known in the art that software can be used to

control the PLL. Since Johnson et al discloses a processor for monitoring

holdover conditions and placing the PLL in holdover, it would have been

obvious to one skilled in the art to incorporate a machine readable medium

for storing instructions based on designer's choice and to control the

system to perform the required instructions or tasks so to provide better and more efficient synchronization of the input signals.

    d. **Claim 15** recites similar claims as claims 1 and 10. Such claims are rejected as stated in claims 1 and 10.

4. **Claims 16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al (US Patent No.: 4849993) in view of McCullagh et al (US Publication No.: 20020022465), further in view of Ham, III (US Publication No.: 20020080901), further in view of Baydar et al (US Publication No.: 20020097743).

    a. **Claim 16** inherits all the limitations of claim 1 and 10 but claims 1 and 10 does not teach a shelf backplane. Baydar et al discloses a shelf backplane and a plurality of shelf elements coupled to the shelf backplane comprising a synchronization of the plurality of shelf elements (Fig. 6, labels 26 and 28, Fig. 7, labels 26 and 28 and Fig. 8), wherein the timing circuit provides a synchronization timing signal to a shelf-plane (Fig. 8, labels 72 and 83 and Fig. 6, labels 26 and 28) and inherently discloses the synchronization timing signal is derived from the first timing signal. (Fig. 8, label 83, page 8, paragraphs [0147][0148][0149], page 9, paragraph [0161] and page 1 O, paragraph [0164]) It would be obvious to one skilled in the art to incorporate a shelf backplane into Johnson et al's invention to allow transmission and reception from other subscribers with different service formats. (page 2, paragraph [0016])

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 17,20,21,22,24,25,30,31,32** are rejected under 35 U.S.C. 102(b) as being

anticipated by Johnson et al (US Patent No.: 4849993).

a. **Claim 17**,

i. Johnson et al discloses

- "generating the timing signal from a reference clock signal in a phase

locked loop" (Fig. 2 shows a phase locked loop, wherein the reference

clock signal is label 10 and the timing signal is label 28)

- "monitoring a status message from a source of the reference clock

signal indicative of a quality level of the reference clock signal" (Fig. 2,

label 26, Col. 5, lines 20-32 discloses the input frequency signal is

checked to determine if the reference signal is within the range. If not,

whether falling below or above the range, the PLL will be placed in

holdover. Fig. 2, label 10 shows the status message is based on the

reference clock signal.) and

- "placing the phase locked loop in a holdover condition if the quality level

indicated by the status message is below a target level, wherein the

method is performed in the order presented" (Col. 5, lines 20-32

discloses the input frequency signal is checked to determine if the

reference signal is within the range. If not, whether falling below or

above the range, the PLL will be placed in holdover.)

- "wherein the target level is an expected quality level of the phase
  locked loop in the holdover condition". (Col. 5, lines 20-32, Col. 4, lines
  36-43 discloses the clock holdover circuit can have a stratum 3 clock
  signal, wherein stratum 3 determine the range for comparison as
  disclosed in Col. 5.)

b. **Claim 20**, Johnson et al discloses "the expected quality level is a Stratum 2

level". (Col. 4, lines 36-43 indicates the Stratum level and the range in which the

Stratum level would indicate the input signal.)

c. **Claim 21**, Johnson et al discloses "placing the phase locked loop in the

holdover condition if the quality level indicated by the status message is below

the target level occurs when the reference clock signal is valid". (Col. 5, lines

20-32 discloses the input frequency signal is checked to determine if the

reference signal is within the range. If not, whether falling below or above the

range, the PLL will be placed in holdover. The column also discloses the

monitor checks for validity of the signal.)

d. **Claims 22,32,**

    i.   Johnson et al discloses

- "generating the timing signal from a reference clock signal in a phase
  locked loop, wherein the reference clock signal is selected from the

group consisting of a primary reference clock signal and at least one

secondary reference clock signal" (Fig. 2 shows a phase locked loop,

wherein the reference clock signal is label 10 and the timing signal is

label 28. Col. 6, lines 12-35 discloses selecting a reference signal.)

- "monitoring status messages received from respective sources of the

  primary reference clock signal and the at least one second reference

  clocks signal indicative of a quality level of the primary reference clock

  signal and the at least one secondary reference clock signal" (Col. 6,

  lines 12-35 discloses selecting a reference signal. The monitor would

  determine the accuracy of reference 10a and 10b. Fig. 3, label 10a and

  10b are used to determine the status of the PLL. Fig. 2, label 10 shows

  the status message is based on the reference clock signal. Fig. 3a,

  labels 58,69 shows the status message, ref fail, is received by the

  controller, label 69, for controlling the switch, label 30, wherein the

  switch controller is part of the processor found in Fig. 2, label 10

  (monitor).) and

- "placing the phase locked loop in a holdover condition if the quality level

  indicated by each status message is below a target level regardless of

  a validity of rely reference clock signal, wherein the method is

  performed in the order presented". (Col. 6, lines 20-40 discloses the

  monitor component checks for accuracy of the signal prior to selecting

10a or 10b. Col. 5, lines 20-32 indicates if the system is not within the

desired range, the system will go into holdover.)

e. **Claim 24**, Johnson et al discloses "maintaining the phase locked loop in the

holdover condition until at least one of the reference clock signals is valid and

has a status message indicating a quality level at or above the target level".

(Col. 5, lines 20-32 discloses the input frequency signal is checked to determine

if the reference signal is within the range. If not, whether falling below or above

the range, the PLL will be placed in holdover. The column also discloses the

monitor checks for validity of the signal.)

f. **Claim 25**, Johnson et al discloses "the phase locked loop is maintained in the

holdover condition for a predetermined period after a reference clock signal

having a valid status has a status message indicating a quality level at or above

the target level". (Col. 5, lines 20-32 discloses the input frequency signal is

checked to determine if the reference signal is within the range. If not, whether

falling below or above the range, the PLL will be placed in holdover. The

column also discloses the monitor checks for validity of the signal.)

g. **Claim 30**,

i. Johnson et al discloses

- "generating the timing signal from a reference clock signal in a phase

locked loop" (Fig. 2, label 28)

- "monitoring a status message received from a source of the reference

  clock signal indicative of a quality level of the reference clock signal"

  (Fig. 2, label 25, Col. 5, lines 20-32) and

- "placing the phase locked loop in a holdover condition if the quality level

  indicated by the status message is below a target level, wherein the

  method is performed in the order presented". (Col. 5, lines 20-32

  discloses the input frequency signal is checked to determine if the

  reference signal is within the range. If not, whether falling below or

  above the range, the PLL will be placed in holdover. Fig. 3a, labels

  58,69 shows the status message, ref fail, is received by the controller,

  label 69, for controlling the switch, label 30, wherein the switch

  controller is part of the processor found in Fig. 2, label 10 (monitor).)

h. **Claim 31**, Johnson et al discloses "placing the phase locked loop in the

   holdover condition if the quality level indicated by the status message is below

   the target level occurs when the reference clock signal is valid". (Col. 5, lines

   20-32 discloses the input frequency signal is checked to determine if the

   reference signal is within the range. If not, whether falling below or above the

   range, the PLL will be placed in holdover. The column also discloses the

   monitor checks for validity of the signal.)

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

7. A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then

the shortened statutory period will expire on the date the advisory action is mailed,

and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the

mailing date of the advisory action. In no event, however, will the statutory period

for reply expire later than SIX MONTHS from the mailing date of this final action.

      Any inquiry concerning this communication or earlier communications from the
examiner should be directed to LINDA WONG whose telephone number is (571)272-
6044. The examiner can normally be reached on 9-5.
      If attempts to reach the examiner by telephone are unsuccessful, the examiner's
supervisor, David Payne can be reached on (571) 272-3024. The fax phone number for
the organization where this application or proceeding is assigned is 571-273-8300.
      Information regarding the status of an application may be obtained from the
Patent Application Information Retrieval (PAIR) system. Status information for
published applications may be obtained from either Private PAIR or Public PAIR.
Status information for unpublished applications is available through Private PAIR only.
For more information about the PAIR system, see http://pair-direct.uspto.gov. Should
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system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Linda Wong
11/2/2009

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